COUNTER - CARD ZIB 1177

General Description

The counter card type ZIB 1177 was designed to interface directly with the PC's (conventional, IBM standard) internal bus through any available expansion slot. Major feature of this card are **8 programmable 32-bit binary up/down counters.** The use of Schmitt-triggered CMOS inputs allows reliable operation in noisy envirements. The counters are used for **measurement of length** by incremental encoders with two channels output. If it is nessary each of the 32-bit counter may be programmed as two 16-bit counters. By this way 16 independent 16-bit binary counters are available.

The counters can also be used for event counting. This is done by appropriate programming.

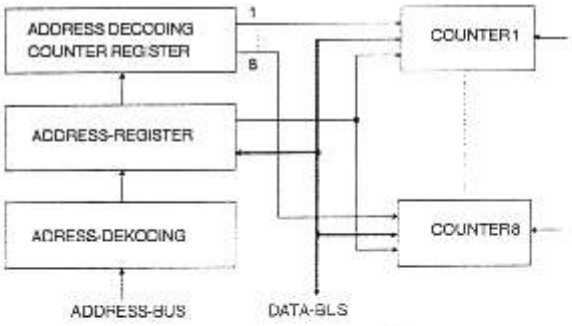


Fig. 1

The block diagramm of the counter card ZIB1177 is shown in figure 1. Each of the 8 counters may be used in different operating modes. The operating modes are selectable by programming.

In most cases the binary counter will be programmed for up/down counting. This operating mode is nessary for measurement of length or for positioning. Each counter is supplied with two inputs for signals of incremental encoders and a hardware reset input for reference pulses. Incoming pulses for measurement of length must be 90 degrees out of phase. Each counter has an internal 4/2/1-fold decoder (programmable), up/down detection, and a 32-bit output latch register.

An internal control logic is provided for correct reading of the counter position when transferring datas into the output latch register.

Input voltage level of the input pulses of the counter card ZIB1177 (respective the counter) are selectable by exchangable resistor networks. By this way the input voltage level can be adjusted between 5V and 24V. If the counter card is ordered, the desired input voltage level should also be ordered. The ordered input level will be set in factory.

Base Address Selection

The card is controlled through the input/output (I/O) ports. The I/O port base address is selectable via an 8 position dip switch "S1".

DIP SWITCH "S1"	ADDRESS
1	200H
2	100H
3	080H
4	040H
5	020H
6	010H
7	008H
8	004H

Note: ON = 0, OFF = 1

The card needs two addresses, base address and base address + 1. The addresses may be placed within the whole I/O address range (from 0 to 3FCH). Attention must be paid, that the selected I/O addresses of the card are not used by an other interface. The factory setting is 100H.

Counter Addressing

The card was designed for indirekt addressing. For writing counter commands and/or reading datas of the counters, the base address will be used. The addresses for programming the counters must be written into an additional internal address register. The address of the internal address register

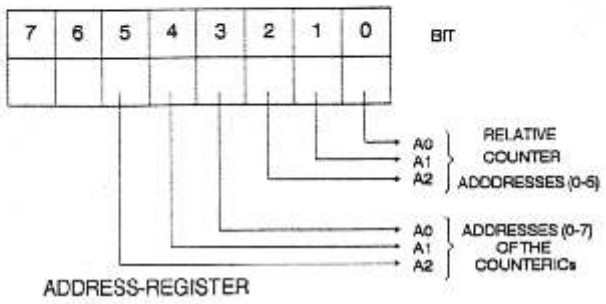


Fig. 2

is the I/O adress "base address + 1". The address register determines which counter and which register of the counter is addressed. Figure 2 shows the address register. The lower 3 bits of the address register are used for addressing the relative counter register. The bits 3 to 5 will address the counter IC itself. Bit 6 and 7 will have no function.

Internal Structure Of Counter ICs

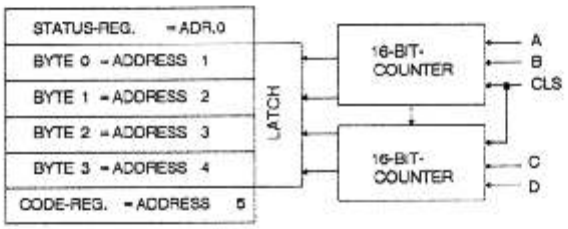


Fig. 3

Each of the 8 counter ICs has 5 register with the relative addresses 0 to 5 (see figure 3).
Register 0 is used for latching the counter position. Latching is performed by an write command to address 0. The latched counter position is stored in the register 1 to 4 of the counter.
Register 5 is the code register. This register is used for programming the operating mode.

Installing Up/down Counting

Before using the counter card the counter ICs must set to the desired operating mode. This is done by writing the appropriate code word into the code register (5). The mode definition format is shown in figure 4. For the most used mode, 32-bit up/down counting and quadrature decoder function the code word is 00H. Bit 0 and bit 2 are used for programming 1/2/3/4-fold counting. Hysterese of one digit is enabled with bit 5 = 1. Bit 4 = 1 enables 2 x 16-bit counter.

Direct Mode

If event counting is desired, bit 7 must be "1". In this case bit 5 determines the counting direction (1 = upwards, 0 = downwards). Input "A" of the counter is the counting input, input "B" has the function of a gate. High level at this input will inhibit counting.

Register Adresses Of Counter IC

CS	A2	A1	A0	READ	WRITE
0	0	0	0	Status - Register	Strobe
0	0	0	1	Byte 0	Byte 0
0	0	1	0	Byte 1	Byte 1
0	0	1	1	Byte 2	Byte 2
0	1	0	0	Byte 3	Byte 3
0	1	0	1		Code - Register
0	1	1	0		
0	1	1	1		

For detailed application refer to the Siemens S360 B114 produkt literature.

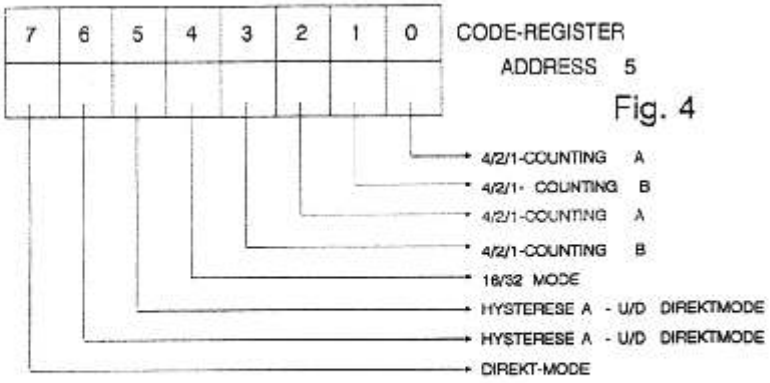


Fig. 4

Reading The Counter Position

This is done with writing 00H to the relative counter address 0. By this command the counter position is latched. The latched counter position will be received by reading byte 0 (relative counter address 1), byte 1 (relative counter address 2), byte 2 (relative counter address 3), and byte 3 (relative counter address 4).

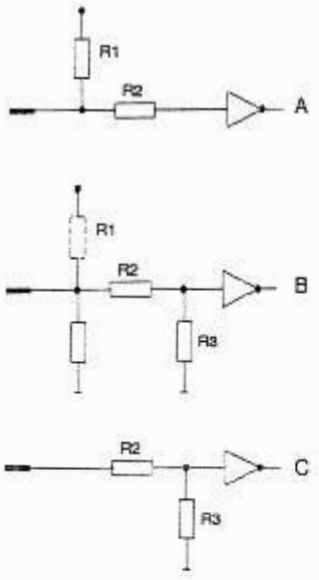
Setting Counter Position

Each counter can also be set to a preselect value by writing the desired value to the relative addresses 1 to 4.

Counter Reset

Each counter may be set to zero per software. In this case the value 00H must be written into the relative registers 1 to 4.

Beside the software reset there is a hardware reset for each of the 8 counters. Hardware reset can be done via the inputs "CLS" at the card connector. Low level at the "CLS"-input means reset. Reset pins not connected means also reset (because of the resistor networks on the card. To enable counting, the reset inputs must be set to high level by an external signal.



Inputs

The counting and reset inputs use resistor networks to perform voltage divider for the input voltage. By this way the level of the input signal can be adjusted to the desired input level. Additionally the inputs are protected against overvoltage.

For adjusting input voltage levels there are the resistor networks R1,R2, and R3 (see figure 5). These resistor networks are exchangeable. The resistor values will be calculated for the desired input voltage. CMOS Schmitt-trigger allows reliable operation in noisy envirements.

The CMOS-ICs have a high input impedance and an input threshhold of 2.5V. At 24V input levels input impedances of 100k may be realized. Merely at high counting frequencies it is recommended to use resistances of lower values (in the range of 1 to 10k). High values of input resistances will reduce input frequencies because of the filter consisting of resistor networks and input capacitances of the CMOC-ICs.

When ordering a counter card, it is recommended to specify the desired input level and the desired input frequencies. The resistors networks are then set to the accomodate values in the factory.

If no input levels are specified, the values set in the factory are (see figure 5A) R1 = 1K, R2 = 10K, for input pulses of 5V.

Connector Pin Assignment

Counter	A1	B1	C1	D1	CLR
1	02	04	07	06	19
2	21	20	05	18	03
3	10	11	30	17	12
4	27	16	08	09	28
5	46	43	13	29	33
6	14	44	15	26	47
7	49	48	23	50	22
8	32	31	25	45	24

Ground	41/40/39/38
+ 5 V	34 (internal)

Produkt Specifications

Inputs	
Input Voltage level	5V to 24V adjustable
Counter reset	Low Active
Dimensions	190x108mm
Weight	220g
Power Suppy	5V/1.0A

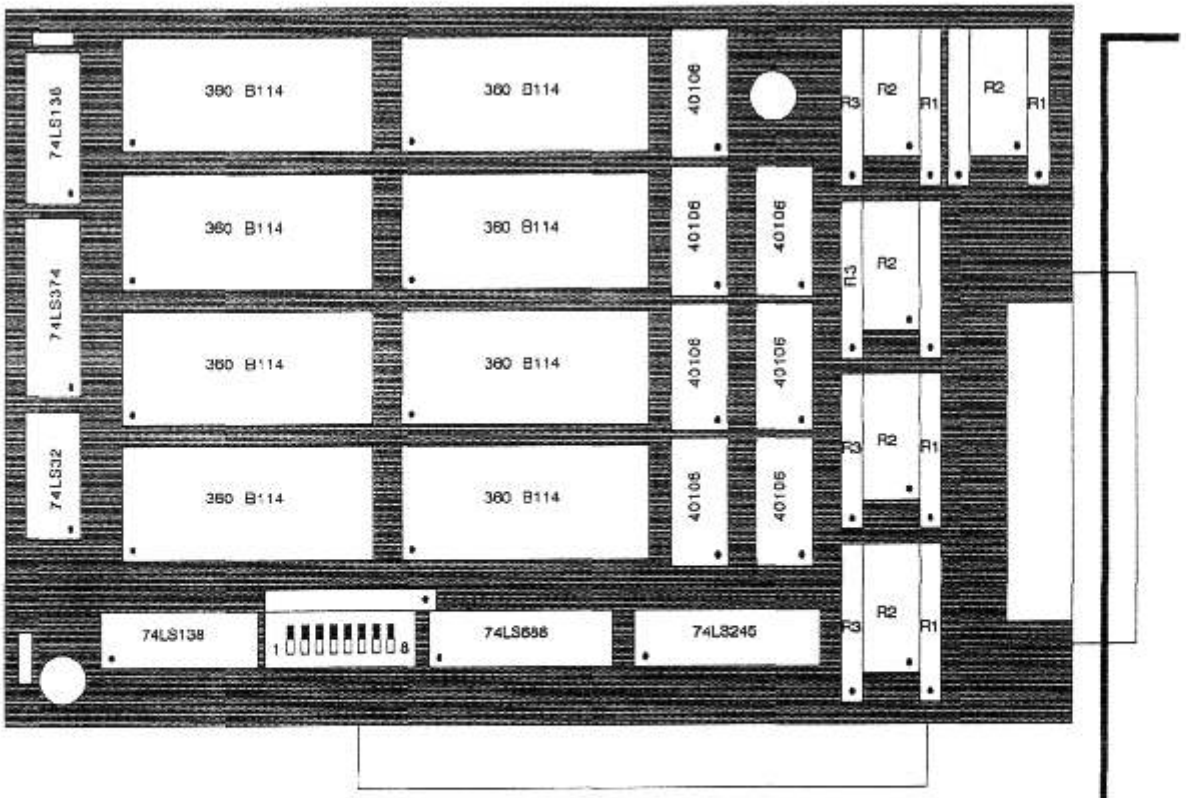
Programming Hints

The counter can be programmed also for 3-fold counting. This counting mode is not documented by the manufacterer. The programming hints for the code words are shown below.

COUNTING MODE

	Bit 2	Bit 0
4-fold	0	0
3-fold	0	1
2-fold	1	0
1-fold	1	1

Bit 7 = "1" will desaktivate Bit 2 and Bit 0



BOARD LAYOUT